CLAIMS

1. A registered memory module, comprising:

a register receiving a plurality of signals at respective input terminals, the register storing the input signals responsive to a transition of an internal clock signal applied to a clock terminal when an enable signal is active, the register having output terminals on which the stored input signals are present;

a plurality of memory devices coupled to the output terminals of the register, each of the memory devices being selected by a respective select signal being active; and

a logic circuit receiving the select signals for the memory devices and applying the enable signal to the register, the logic circuit being structured to make the enable signal active responsive to any of the select signals being active and to make the enable signal inactive response to none of the select signals being active.

2. The registered memory module of claim 1 wherein the register comprises a plurality of flip-flops each having a data terminal receiving a respective one of the input signals and a clock terminal receiving the clock signal.

3. The registered memory module of claim 2 wherein each of the flip-flops includes an enable terminal coupled to receive the enable signal from the logic circuit, the flip-flops latching the input signals applied to respective data terminals responsive to the enable signal being active.

4. The registered memory module of claim 3 wherein the logic circuit comprises a NAND gate.

5. The registered memory module of claim 1 wherein the register comprises:

a plurality of logic gates each having a first input terminal to which a respective one of the input signals is coupled and a second input terminal to which the enable signal is coupled, each of the logic gates having an output terminal; and

a plurality of flip-flops each having a data terminal coupled to the output terminal of a respective one of the logic gates and a clock terminal receiving the clock signal.

6. The registered memory module of claim 5 wherein the logic circuit comprises an AND gate.

7. The registered memory module of claim 5 wherein each of the logic gates comprise an OR gate.

8. The registered memory module of claim 1 wherein each of the memory devices comprise a dynamic random access memory ("DRAM") device.

9. The registered memory module of claim 8 wherein each of the DRAM devices comprise a synchronous DRAM device.

10. The registered memory module of claim 1 wherein the memory module further receives a clock enable signal, and wherein the clock enable signal is stored in the register.

11. The registered memory module of claim 1 wherein the input signals comprise address signals.

12. The registered memory module of claim 1 wherein the input signals further comprise the select signals.

13. The registered memory module of claim 1 wherein the logic circuit comprises a logic gate.

14. The registered memory module of claim 13 wherein the logic circuit comprises a NAND gate.

15. The registered memory module of claim 13 wherein the logic circuit comprises an AND gate.

16. A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller; and

at least one registered memory module coupled to the CPU through the system controller, the at least one registered memory module comprising:

a register receiving a plurality of signals at respective input terminals, the register storing the input signals responsive to a transition of an internal clock signal applied to a clock terminal when an enable signal is active, the register having output terminals on which the stored input signals are present;

a plurality of memory devices coupled to the output terminals of the register, each of the memory devices being selected by a respective select signal being active; and

a logic circuit receiving the select signals for the memory devices and applying the enable signal to the register, the logic circuit being structured to make the enable signal active responsive to any of the select signals being active and to make the enable signal inactive response to none of the select signals being active.

17. The computer system of claim 16 wherein the register comprises a plurality of flip-flops each having a data terminal receiving a respective one of the input signals and a clock terminal receiving the clock signal.

18. The computer system of claim 17 wherein each of the flip-flops includes an enable terminal coupled to receive the enable signal from the logic circuit, the flip-flops latching the input signals applied to respective data terminals responsive to the enable signal being active.

19. The computer system of claim 18 wherein the logic circuit comprises a NAND gate.

20. The computer system of claim 16 wherein the register comprises:

a plurality of logic gates each having a first input terminal to which a respective one of the input signals is coupled and a second input terminal to which the enable signal is coupled, each of the logic gates having an output terminal; and

a plurality of flip-flops each having a data terminal coupled to the output terminal of a respective one of the logic gates and a clock terminal receiving the clock signal.

21. The computer system of claim 20 wherein the logic circuit comprises an AND gate.

22. The computer system of claim 20 wherein each of the logic gates comprise an OR gate.

23. The computer system of claim 16 wherein each of the memory devices comprise a dynamic random access memory ("DRAM") device.

24. The computer system of claim 23 wherein each of the DRAM devices comprise a synchronous DRAM device.

25. The computer system of claim 16 wherein the memory module further receives a clock enable signal, and wherein the clock enable signal is stored in the register.

26. The computer system of claim 16 wherein the input signals comprise address signals.

27. The computer system of claim 16 wherein the input signals further comprise the select signals.

28. The registered memory module of claim 16 wherein the logic circuit comprises a logic gate.

29. The registered memory module of claim 28 wherein the logic circuit comprises a NAND gate.

30. The registered memory module of claim 28 wherein the logic circuit comprises an AND gate.

31. A method of accessing a plurality of memory devices coupled to a register that receives a plurality of input signals, the method comprising:

determining whether or not a memory access is directed to any of the memory devices;

periodically storing the input signals in the register responsive to determining that the memory access is directed to any of the memory devices; and

refraining from periodically storing the input signals in the register responsive to determining that the memory access is not directed to any of the memory devices; and

coupling the stored input signals to the memory devices.

32. The method of claim 31 wherein respective select signals are applied to each of the memory devices to enable their operation, and wherein the act of determining whether or not a memory access is directed to any of the memory devices comprises examining the select signals and determining if any of the select signals have a predetermined state.

33. The method of claim 31 wherein the acts of periodically storing the input signals in the register and refraining from periodically storing the input signals in the register comprise:

coupling the input signals to the register through respective logic gates;

enabling the logic gates responsive to determining that the memory access is directed to any of the memory devices; and

disabling the logic gates responsive to determining that the memory access is not directed to any of the memory devices.

34. The method of claim 31 wherein the register stores the input signals responsive to a clock signal when the register is enabled by an enable signal, and wherein the acts of periodically storing the input signals in the register and refraining from periodically storing the input signals in the register comprise:

coupling the input signals to the register;

enabling the register responsive to determining that the memory access is directed to any of the memory devices; and

disabling the register responsive to determining that the memory access is not directed to any of the memory devices.

35. The method of claim 31 wherein the act of periodically storing the input signals comprises periodically storing address signals.

36. The method of claim 31 wherein each of the memory devices comprises a dynamic random access memory ("DRAM") device.

37. The method of claim 36 wherein each of the DRAM devices comprises a synchronous DRAM device.

38. The method of claim 31 wherein the act of periodically storing the input signals comprises periodically storing respective select signals selecting the memory devices for memory accesses.

39. In a registered memory module having a register for storing input signals responsive to a clock signal and coupling the stored input signals to a plurality of memory devices in the module, a method of reducing the power consumed by the registered memory module, comprising:

determining whether or not a memory access is directed to any of the memory devices in the module;

enabling the register to periodically store the input signals responsive to determining that the memory access is directed to any of the memory devices; and

disabling the register from periodically storing the input signals responsive to determining that the memory access is not directed to any of the memory devices.

40. The method of claim 39 wherein respective select signals are applied to each of the memory devices to enable their operation, and wherein the act of determining whether or not a memory access is directed to any of the memory devices comprises examining the select signals and determining if any of the select signals have a predetermined state.

41. The method of claim 39 wherein the acts of enabling and disabling the register comprise:

coupling the input signals to the register through respective logic gates;

enabling the logic gates responsive to determining that the memory access is directed to any of the memory devices; and

disabling the logic gates responsive to determining that the memory access is not directed to any of the memory devices.

42. The method of claim 39 wherein the act of enabling the register to periodically store the input signals comprises periodically enabling the register to periodically store address signals.

43. The method of claim 39 wherein each of the memory devices comprises a dynamic random access memory ("DRAM") device.

44. The method of claim 43 wherein each of the DRAM devices comprises a synchronous DRAM device.

45. The method of claim 39 wherein the act of periodically storing the input signals comprises periodically storing respective select signals selecting the memory devices for memory accesses.